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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,489	04/15/2004	Frederic Reblewski	003921.00008	6574

22907 7590 03/04/2009

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
03/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,489	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 15-24* is/are pending in the application.

4a) Of the above claim(s) *19-24* is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-10* is/are allowed.

6)☒ Claim(s) *15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *19-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-2, 4-10, 15-24 has/have been presented for examination based on amendment filed on 03 April 2008.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/01/2008 has been entered.
3. Claim(s) 1, 4, 6, 8 is/are amended.
4. Claim(s) 15-24 is/are new.
5. Claim(s) 3 is cancelled and claims 11-14 were previously cancelled.
6. Claims 1-10 are allowable and all rejections for them are withdrawn.
7. Claim(s) 15-18 are newly rejected under 35 USC § 102.
8. Claims 19-24 are presented with restriction by original presentation.
9. The arguments submitted by the applicant have been fully considered. Claims 15-18 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

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Response to Applicant's Remarks & Examiner's Withdrawals

10. Applicant's arguments are found to be persuasive that Barbier memory element 112 is not explicitly used to program the crossbar switches. In fact none of the three crossbar switches are programmed with the memory disclosed in Barbier. Although programmable crossbar switches are well known in the art, claims 1, 4, 6, and 8 disclose system/apparatus which if mapped to Barbier lacks the programmable crossbar and would lead to change in functionality of Barbier if combined with what is known in the art (programmable crossbar switches).

Claim Interpretation

Claim 18 discloses:

> "wherein the simulation processors are configured to execute an instruction to perform a simulation of a function, the instruction comprising wait data reflecting a time to wait before executing a next instruction…"

This limitation is a functional limitation in an apparatus claim which does not seem to define the apparatus, thus does not constitute a limitation which is given patentable weight.

Election/Restrictions

11. Newly submitted claim19-24 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The claimed invention claims 1-18 is directed towards a system/apparatus of reconfigurable interconnect network comprising of various interconnect and simulation processor structures, whereas claims 19-24 seem to be directed towards use of the claimed reconfigurable interconnect network. The use of the reconfigurable interconnect

network is a independent invention as it specifies a particular sequence in which the reconfigurable interconnect network is used in view of numerous other ways reconfigurable interconnect network can be used by one skilled in the art.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 19-24 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Allowable Subject Matter

12. Although reasons for allowance are briefly presented in the Response to Applicant's Remarks & Examiner's Withdrawals section, full reasons are withheld until the other issues in this application are resolved.

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Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claim 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,545,505 issued to Chan et al.

Regarding Claim 15

Chan teaches a reconfigurable interconnect network comprising (Chan: Col.1 Lines 22-25; Col.5 Lines 8-16): a plurality of simulation processors having a respective plurality of outputs and a respective plurality of inputs (Chan: Fig.1 and Logic CPLD as simulation processors; Alternately also see Fig.11 for more complex layout); a reconfigurable interconnect stage having a plurality of inputs configured to connect to the plurality of outputs from the simulation processors (Chan: Fig.1) and further having a plurality of outputs configured to connect to the plurality of inputs of the simulation processors (Chan: Fig.1 and associated text); and memory, wherein the reconfigurable interconnect network is configured to dynamically re-configure the reconfigurable interconnect stage in accordance with a content of the memory (Chan: Col.5 Lines 8-16).

Regarding Claim 16

Chan teaches wherein the reconfigurable interconnect network is configured to dynamically re- configure the reconfigurable interconnect stage according to a sequence of simulation events (Col.1 Lines 36-45; Col.9 Lines 21-33) as programmable as non-volatile memory element stores the interconnect (PIM) configuration.

Regarding Claim 17

Chan teaches wherein the plurality of processor elements are configured to simulate different functions according to a sequence of simulation events (Chan: Fig.10A-C & 11 and associated text), and wherein the reconfigurable interconnect network is configured to dynamically re- configure the reconfigurable interconnect stage according to the sequence of simulation events (Chan: Col.1 Lines 36-45; Col.9 Lines 21-33).

Regarding Claim 18

Chan teaches a reconfigurable interconnect network comprising (Chan: Col.1 Lines 22-25; Col.5 Lines 8-16): a plurality of simulation processors having a respective plurality of outputs and a respective plurality of inputs (Chan: Fig.1 and Logic CPLD as simulation processors; Alternately also see Fig.11 for more complex layout); and a reconfigurable interconnect stage having a plurality of inputs configured to connect the plurality of outputs from the simulation processors and further having a plurality of outputs configured to connect to the plurality of inputs of the simulation processors (Chan: Fig.1 and associated text).

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akash Saxena/
Examiner, Art Unit 2128

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128